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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/499,599	02/07/2000	Yutaki Aoki	00068/LH	1490

1933 7590 05/02/2002

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EXAMINER	
HA, NATHAN W	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/02/2002

due Aug. 2, 02

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/499,599	AOKI ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 3, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohta et al., hereinafter Ohta (US. 6,337,517, newly cited).

5. In regard to claims 1 and 6, in fig. 11, Ohta discloses a semiconductor device 1, comprising

a semiconductor substrate 2 having a circuit element formation and a plurality of connection pads 5, the plurality of connection pads including

1. at least one first connection pad which is part of metal 5, on the right side of figure 11, connected to a barrier layer, also 5, provided on the circuit element formation region through a first insulating film 6 interposed therebetween, the barrier layer comprising a first conductor layer, which covers the circuit element formation region and which electrically connected to at least one first straight-shaped columnar electrode, see fig. 11 for detail since these elements were not numbered explicitly.

2. at least one second connection pad 5, at the left side, electrically connected to a second conductor layer on the barrier through a second insulating film 6 interposed therebetween, the second conductor layer being connected to at least one second straight-shaped columnar electrode 7.

In regard to claim 3, see fig. 11.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et al. in view of Koshsiek (previous applied).

Ohta et al. shows most aspects of the instant invention (paragraph 2) but does not show a barrier layer including one of ground potential layer, a power supply potential layer and an electromagnetic wave absorption layer. In figure 2, Koshsiek shows conductor track 3 is connected at a suitable point to the ground (column 2, lines 13, 14). The motivation for doing so would have been provide a metal layer which is connected to ground potential and covers the whole surface in order to avoid a crosstalk between the conductor tracks of the two aforementioned wiring levels (column 1, lines 39 to 42).

Therefore, it would be obvious to one of ordinary skill in the art to combine the ground potential layer to the semiconductor device of Ohta et al. as taught by Koshsiek in order to avoid a crosstalk between the conductor tracks of the two aforementioned wiring levels.

4. Claim 4 is rejected under 35 U.S C 103 (a) as being uppatentable over Ohta et al. in view of Suzuki et al. (previous applied).

Ohta et al. shows most aspects of the instant invention (paragraph 2) but do not show the planar circuit element adhered to the lower surface of the semiconductor substrate. In figure 10, Suzuki et al. disclose attaching the circuit component 13 to the lower substrate 11. The purpose of doing this would have been to transfer the heat

generated in the circuit component to the mother board without passing through the substrate (column 1, lines, 66-67 to column 2, line 1).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the semiconductor device of Ohta et al. by attaching a circuit component to the lower surface of semiconductor substrate as taught by Suzuki et al. to transfer the heat generated in the circuit component to the mother board without passing through the substrate.

5. Claim 5 is rejected under 35 U.S C 103 (a) as being uppatentable over Ohta et al. in view of Suzuki et al. and further in view of Noma et al. (U.S. 5,818,079, previous applied).

Ohta et al. in view of Suzuki et al. show most aspects of the instant invention (paragraph 4) but do not disclose the planar circuit element including one of a film-like capacitor and a film-like resistor. Noma et al. teaches a semiconductor device having a thin-film capacitor with the lower electrode 53A, the upper electrode 55A, and a capacity insulating film 54A (column 1, lines 55-62). The purpose for doing so would have provided a high integration of the semiconductor integrated circuit device, the chip area have been reduced by the high integration in order to get smallsized information communication equipment and to lower the cost (Column 1, line 1821).

Therefore, it would have been obvious to one of ordinary skill in the art to form a thin- film capacitor in the semiconductor device of Ohta et al. in view of Suzuki et al. as taught by Noma et al. to get small- sized information communication equipment and to lower the cost.

6. Claims 8,13, 15 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et al. in view of Brotherton (previous applied).

Ohta et al. show most aspects of the instant invention (paragraph 2) but do not show a thin-film circuit element provided on the first insulating film. Referring to figure 3, Brotherton discloses forming thin- film circuit elements 36 having a conductive layer 1 with an insulating film 3 interposed (column 5, lines 19-20). The motivation of doing so have been desired for high mobility, for example, for fast switching applications, crystsalline semiconductor regions (column 1, lines 29-30).

Therefore, it would have been obvious to one of ordinary skill in the art to form a thin- film element provided on the first insulating film of semiconductor device of Ohta et al. as taught by Brotherton where high mobility is desired.

Examiner notes that it is obvious to duplicate the first barrier layer in the semiconductor device of the instant invention to get the second barrier layer as claimed in claim 13 to increase the capacity of semiconductor device.

7. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et al. in view of Brotherton, and further in view of Kohsiek.

Ohta et al. in view of Brotherton show most aspects of the instant invention (paragraph 6) but do not show a barrier layer including one of a ground potential layer, a power supply potential layer and an electromagnetic wave absorption layer. In figure 2, Koshsiek shows conductor track 3 is connected at a suitable point to the ground column 2, lines 13, 14). The motivation for doing so would have been provided a metal layer which is connected to ground potential and covers the whole surface in order to avoid a

cross-talk between the conductor tracks of the two aforementioned wiring levels (column 1,lines 39 to 42).

Therefore, it would have been obvious to one of ordinary skill in the art to combine the ground potential layer to the semiconductor device of Ohta et al. in view of Brotherton as taught by Koshsiek to avoid a cross-talk between the conductor tracks of the two aforementioned wiring levels.

In regard to claim 15, see the discussion above regarding to claim 9.

8. Claims 10 and 16 are rejected under 35 U.S. C. 103(a) as being unpatentable over Ohta et al. in view of Brotherton as applied to the claim 6 above, and further in view of Noma et al.

Ohta et al. in view of Brotherton show most aspects of the instant invention (paragraph 6) but do not show a thin- film circuit element including one of a thin-film inductor, a thin-film transformer, a thin-film capacitor, a thin -film SAW filter, a microstrip line, and a MMIC (Microwave Monolithic Integrated Circuit). In figure 11, Noma et al. teach a semiconductor device having a thin-film capacitor with the lower electrode 53A, the upper electrode 55A, and a capacity insulating film 54A (column 1, lines 55,56,61 and 62). The purpose for doing so would have provided a high integration of the semiconductor integrated circuit device, the chip area have been reduced by the high integration in order to get small- sized information communication equipment and to lower the cost (Column 1, line 18- 21).

Therefore, it would have been obvious to one of ordinary skill in the art to form a thin- film capacitor to the semiconductor device of Ohta et al. in view of Brotherton as

taught by Noma et al. to get small- sized information communication equipment and to lower the cost.

9. Claims 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et al. in view of Brotherton as applied to claim 6 above, and further in view of Suzuki.

Ohta et al. in view of Brotherton show most aspects of the instant invention (paragraph 6) but do not show a planar circuit element adhered to the lower surface of the semiconductor substrate. In figure 10, Suzuki et al. disclose attaching the circuit component 13 to the lower substrate 11. The purpose of doing this would have been to transfer the heat generated in the circuit component to the mother board without passing through the substrate (column 1, lines, 66-67 to column 2, line 1).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the semiconductor device of Ohta et al. in view of Brotherton by attaching a circuit component to the lower surface of semiconductor substrate as taught by Suzukii et al. to transfer the heat generated in the circuit component to the mother board without passing through the substrate.

10. Claims 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et al. in view of Brotherton and Suzuki et al. as applied to claim 11 above, and further in view of Noma et al.

Ohta et al. in view of Brotherton and Suzuki et al. show most aspects of the instant invention (paragraph 9) but do not show the planar circuit element including one of a film-like capacitor and a film-like resistor. Noma et al. teach a semiconductor device

having a thin-film capacitor with the lower electrode 53A, the upper electrode 55A, and a capacity insulating film 54A (column 1, lines 55,56,61 and 62). The purpose for doing so would have provided a high integration of the semiconductor integrated circuit device, the chip area have been reduced by the high integration in order to get small-sized information communication equipment and to lower the cost Column 1, line 18-21).

Therefore, it would have been obvious to one of ordinary skill in the art to add a thin-film capacitor to the semiconductor device of Ohta et al. in view of Brotherton and Suzuki et al. as taught by Noma et al. to provide a high integration of semiconductor circuit and get small- sized information communication equipment and to lower the cost.

Response to Arguments

11. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (703) 305-3507. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and 308-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Nathan Ha
April 9, 2002

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Notice of References Cited	Application/Control No. 09/499,599	Applicant(s)/Patent Under Reexamination AOKI ET AL.	
	Examiner Nathan W. Ha	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,337,517	01-2002	Ohta et al.	257/700
	B	US-5,818,079	10-1998	Noma et al.	257/295
	C	US-6,031,293	02-2000	Hsuan et al.	257/698
	D	US-5,928,968	07-1999	Bothra et al.	438/53
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.